Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

an etch stop layer on the substrate overlying the NMOS device and the PMOS device; and

wherein a first one of the NMOS and PMOS devices includes a gate and a first source/drain regions, wherein the first source/drain regions are recessed ~~within the surface, wherein the first source/drain regions are~~ and disposed entirely below the surface of the substrate and wherein the first source/drain regions are recessed such that the etch stop layer overlying the gate and the first source/drain regions extends below an interface of the gate and the surface; and

wherein a second one of the NMOS and PMOS devices includes second source/drain regions at least partially extending above the surface of the substrate, and wherein the etch stop layer imparts a first strain within the first source/drain region and a second strain within the second source/drain region, the first and second strain being different in magnitude.

2. (Original) The semiconductor device of claim 1 wherein:

a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and

a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

3. (Original) The semiconductor device of claim 1 wherein:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.

4. (Original) The semiconductor device of claim 2 wherein:

a wide-spacer one of the NMOS and PMOS devices includes first spacers on opposing sides of an associated one of the first and second gates, the first spacers each extending from the associated gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes second spacers on opposing sides of an associated one of the first and second gates, the second spacers each extending from the associated gate to a second width, wherein the first width is substantially greater than the second width.

5. (Original) The semiconductor device of claim 1 wherein at least one set of the first and second source/drain regions comprises SiGe.

6. (Original) The semiconductor device of claim 1 wherein at least one set of the first and second source/drain regions comprises SiC.

7. (Original) The semiconductor device of claim 6 wherein at least one set of the first and second source/drain regions comprise SiGe.

8. (Original) The semiconductor device of claim 1 wherein the substrate has a <110> crystal orientation.

9. (Original) The semiconductor device of claim 1 wherein the substrate has a <100> crystal orientation.

10. (Original) The semiconductor device of claim 1 wherein the substrate is a silicon-on-insulator substrate.

11. (Original) The semiconductor device of claim 1 wherein the substrate is a bulk silicon substrate.

12. (Original) The semiconductor device of claim 1 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

13. (Original) The semiconductor device of claim 2 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

14. (Original) The semiconductor device of claim 3 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

15. (Canceled)

16. (Currently Amended) A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes:

first source/drain regions recessed within the substrate; and

a first gate interposing the first source/drain regions and having a first gate height over the surface, wherein the first source and drain regions are disposed entirely below an imaginary plane extending from the interface of the first gate and the substrate, and wherein a top surface of the first source/drain region lies below the imaginary plane; and

wherein a second one of the NMOS and PMOS devices includes:

second source/drain regions at least partially extending above the surface, and extending at least partially above the imaginary plane extending from the interface of the second gate and the substrate; and

a second gate interposing the second source/drain regions and having a second gate height over the surface, wherein the first and second gate heights are substantially different, and

an etch stop layer overlying the first gate, the second gate, the first source/drain regions and the second source/drain regions, wherein the etch stop layer extends below the imaginary plane extending from the interface of the first gate and the substrate.

17. (Original) The semiconductor device of claim 16 wherein:

a wide-spacer one of the NMOS and PMOS devices includes first spacers on opposing sides of an associated gate, the first spacers each extending from the associated gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes second spacers on opposing sides of an associated gate, the second spacers each extending from the associated gate to a second width, wherein the first width is substantially greater than the second width.

18. (Original) The semiconductor device of claim 16 wherein at least one set of the first and second source/drain regions comprises SiGe.

19. (Original) The semiconductor device of claim 16 wherein at least one set of the first and second source/drain regions comprises SiC.

20. (Original) The semiconductor device of claim 19 wherein at least one set of the first and second source/drain regions comprises SiGe.

21. (Original) The semiconductor device of claim 16 wherein the substrate has a <110> crystal orientation.

22. (Original) The semiconductor device of claim 16 wherein the substrate has a <100> crystal orientation.

23. (Original) The semiconductor device of claim 16 wherein the substrate is a silicon-on-insulator substrate.

24. (Original) The semiconductor device of claim 16 wherein the substrate is a bulk silicon substrate.

25. (Previously Presented) The semiconductor device of claim 16 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

26. (Previously Presented) The semiconductor device of claim 17 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

27. (Currently Amended) The semiconductor device of claim 16 ~~further comprising an~~ wherein the etch stop layer ~~located over the NMOS and PMOS devices and contributing~~ contributes to the substantial magnitude difference between the first stress in the first source/drain regions and the second stress in the second source/drain regions.

28. (Currently Amended) A semiconductor device, comprising:

an isolation region located in a substrate;

an NMOS device located partially over a surface of the substrate; and

a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;

wherein a first one of the NMOS and PMOS devices includes:

first source/drain regions recessed within the substrate, wherein a first contact coupled to the first source/drain region extends below the surface of the substrate;

a first gate interposing the first source/drain regions and disposed on the surface of the substrate thereby providing a first interface between the substrate and the first gate; and

first spacers on opposing sides of the first gate and each extending from the first gate to a first width; and

wherein a second one of the NMOS and PMOS devices includes:

second source/drain regions at least partially extending above the surface;

a second gate interposing the second source/drain regions an disposed on the surface of the substrate thereby providing a second interface between the substrate and the second gate; and

second spacers on opposing sides of the second gate and each extending from the second gate to a second width, wherein the first and second widths are substantially different; and

an etch stop layer overlying the NMOS and PMOS device wherein the etch stop layer extends below the first interface, wherein the etch stop layer is at least one of a tensile film and a compressive film.

29. (Original) The semiconductor device of claim 28 wherein at least one set of the first and second source/drain regions comprises SiGe.

30. (Original) The semiconductor device of claim 28 wherein at least one set of the first and second source/drain regions comprises SiC.

31. (Original) The semiconductor device of claim 30 wherein at least one set of the first and second source/drain regions comprises SiGe.

32. (Original) The semiconductor device of claim 28 wherein the substrate has a <110> crystal orientation.

33. (Original) The semiconductor device of claim 28 wherein the substrate has a <100> crystal orientation.

34. (Original) The semiconductor device of claim 28 wherein the substrate is a silicon-on-insulator substrate.

35. (Original) The semiconductor device of claim 28 wherein the substrate is a bulk silicon substrate.

36. (Original) The semiconductor device of claim 28 wherein at least one set of the first and second source/drain regions comprises strained source/drain regions.

37. (Currently Amended) The semiconductor device of claim 28 ~~further comprising~~ ~~an~~ wherein the etch stop layer ~~located over the NMOS and PMOS devices and contributing~~ contributes to the substantial magnitude difference between the first stress in the first source/drain regions and the second stress in the second source/drain regions.

38. – 43. (Canceled)

44. (Currently Amended) A method of manufacturing a semiconductor device, comprising:
forming an isolation region located in a substrate;
forming an NMOS device located partially over a surface of the substrate; and
forming a PMOS device isolated from the NMOS device by the isolation region and located partially over the surface;
wherein the forming of a first one of the NMOS and PMOS devices includes:
etching a recesses in the substrate, and forming a first source/drain regions ~~recessed~~ within the recess ~~within the surface~~, wherein the entire first source/drain region is recessed within the surface and lies entirely below the surface; and
wherein the forming of a second one of the NMOS and PMOS devices includes forming second source/drain regions at least partially extending above the surface; and
forming an etch stop layer over the NMOS device and the PMOS device, wherein a portion of the etch stop layer overlies the first source/drain region and extends into the recesses.

45. (Original) The method of claim 44 wherein:

a high-gate one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and having a first height over the surface; and

a low-gate one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and having a second height over the surface, wherein the first height is substantially greater than the second height.

46. (Original) The method of claim 44 wherein:

a wide-spacer one of the NMOS and PMOS devices includes a first gate interposing associated source/drain regions and first spacers on opposing sides of the first gate, the first spacers each extending from the first gate to a first width; and

a narrow-spacer one of the NMOS and PMOS devices includes a second gate interposing associated source/drain regions and second spacers on opposing sides of the second gate, the second spacers each extending from the second gate to a second width, wherein the first width is substantially greater than the second width.

47. – 49. (Canceled)